M 671321/M 671421

2 K × 8 CMOS Dual Port RAM with Interrupt Flag

Description

The M 671321/671421 are very low power CMOS dual port static RAMs organized as 2048 × 8. They are designed to be used as a stand-alone 8 bit dual port RAM or as a combination MASTER/SLAVE dual port for 16 bits or more width systems. The MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need for additional discrete logic.

Master and slave devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by $\overline{CS}$ permits the onchip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8T) memory cell and fabricated with the state of the art 1.0 µm lithography named SCMOS, the M671321/1421 combine an extremely low standby supply current (typ = 1.0 µA) with a fast access time at 35 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5 µW.

For military/space applications that demand superior levels of performance and reliability the M 671321/1421 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

See M 67132/M 67142 specification for AC.DC parameters.

Features

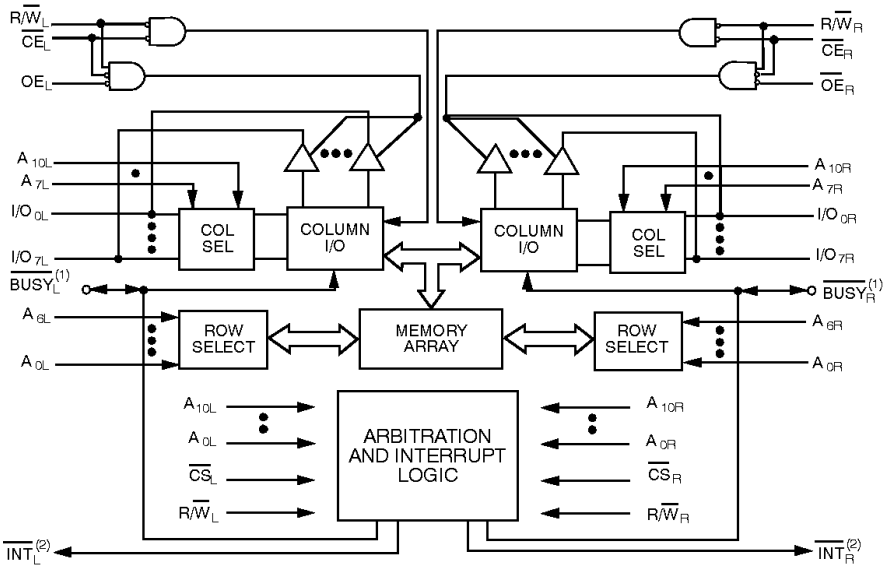
- Fast access time
  35 ns to 55 ns
- 671321L/671421L low power
  671321V/671421V very low power
- Expandable data bus to 16 bits or more using master/slave devices when using more than one device.
- On chip arbitration logic
- $\overline{BUSY}$ output flag on master (M 671321)
- $\overline{BUSY}$ input flag on slave (M 671421)
- $\overline{INT}$ flag for port to port communication
- Fully asynchronous operation from either port
- Battery backup operation : 2 V data retention
- TTL compatible
- Single 5V ± 10 % Power Supply

For 3.3V versions. Please consult sales.

M 671321/M 671421

Interface

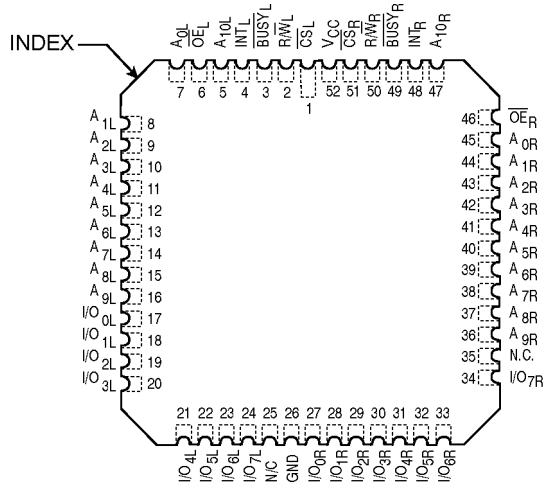
Block Diagram



Notes : 1. M 671321 (MASTER) : $\overline{BUSY}$ is open drain output and requires pull up resistor
M 671421 (SLAVE) : $\overline{BUSY}$ is input
2. Open drain output requires pull up resistor

Pin Configuration

52 PIN PLCC (top view)



Pin Names

LEFT PORT	RIGHT PORT	NAMES
$\overline{CS}_L$	$\overline{CS}_R$	Chip select
$R/\overline{W}_L$	$R/\overline{W}_R$	Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L-9L}	A_{0R-9R}	Address
I/O_{0L-7L}	I/O_{0R-7R}	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
VCC		Power
GND		Ground